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GLITCH AND METASTABILITY CHECKS USING SIGNAL CHARACTERISTICS

RELATED APPLICATIONS

[0001] The present application claims the benefit of U.S. Provisional Application No. 60/497,972 entitled "RELIABILITY-BASED CHARACTERIZATION SYSTEM IN IC/SoC DESIGNS" filed August 25, 2003, the entire contents of which are incorporated herein by reference.

FIELD OF INVENTION

[0002] The present invention generally relates to computer aided methods and tools for designing, simulating, characterizing and verifying integrated circuit (IC) designs, and more particularly to a system and method for verifying and characterizing the noise margin of signals within such designs.

BACKGROUND OF THE INVENTION

[0003] The design of very large-scale integrated (VLSI) circuits using computer aided design (CAD) systems is a very time consuming and computationally intensive process. As the complexity of VLSI circuit design has increased, circuit designers have begun incorporating basic circuit building blocks into circuit designs so that the designers do not need to start from scratch for each design. This design approach is commonly referred to as an intellectual property (IP) based design approach and the basic circuit building blocks are referred to as IP blocks.

[0004] In accordance with system on chip (SOC) technology, a variety of circuit building blocks are incorporated onto a single integrated chip. Each of the building blocks performs a

specific function of an electronic system. The IP building blocks include, but are not limited to, embedded memory, standard cell, I/O devices, analog and system interfaces, etc....

[0005] A timing model including many characterized timing parameters for each IP block that is to be incorporated into a system chip is required by the IC designers. Important timing parameters include setup time, hold time, access time, minimum pulse high and low time, and other I/O pin characteristics. Designers are interested in characterizing and optimizing timing characteristics associated with an IP block design.

[0006] There are two methods of IP block characterization and verification. The first method is based on 'full circuit' simulations. For deep submicron designs, a netlist size of layout-extracted IP blocks could be enormous with a large number of resistors and capacitors. It might be prohibitive to run numerous full circuit simulations with a high-accuracy circuit simulator. The other method is a characterization based on 'critical-path circuit' simulations. Instead of using a full circuit, a small detailed critical circuit including multiple critical paths is used of simulation. The 'critical-path circuits' are built either manually or by software tools for automation, accuracy and performance.

[0007] The simulation results observed during the characterization process are only at the pins of the full circuit or at ports of the 'critical-path circuit'. Reliability issues such as noise margin, glitch, and racing conditions that occur inside the circuit are normally ignored. Accordingly, the timing parameters generated by the simulation may be too optimistic and incorrect.

[0008] Furthermore, the circuit or subcircuit block is viewed as a black-box when the circuit simulation is performed. However, the simulations results observed at the pins cannot detect the above-mentioned reliability issues that can occur inside the circuit. The models based upon simulation and characterization results could be incorrect thereby causing yield and reliability problems.

SUMMARY OF THE INVENTION

[0009] In accordance with the present invention, there is provided a method of performing a glitch check in simulating a circuit. Current maximum and minimum values for optimization parameters of the circuit are determined. The optimization parameters are setup or hold time for the circuit simulations. Next, a signal characteristic for the circuit simulation is determined based on the maximum and minimum optimization parameters. The signal characteristic can be either the height or width of the signal pulse, or the slew time of the signal transition. A current averaged optimization parameter is determined from the current maximum and minimum optimization parameters. A prime criterion parameter is calculated based on the optimization parameters and the signal characteristic value. If the prime criterion parameter converges into a prescribed range, then measurement results from the circuit simulation are parsed.

[0010] However, if the prime criterion parameter does not converge into the prescribed range, then the circuit is simulated based on the current optimization parameter and a new signal characteristic is calculated. Next, the results of the circuit simulation based on the signal characteristic value are determined. The current optimization parameter is set to a new optimization parameter in response to the signal pulse characteristic value. Specifically, the current optimization parameter is set a new optimization parameter that is the maximum value of the optimization parameter if the current optimization parameter and the minimum optimization parameter do not indicate the same status (i.e., one succeeds and the other fails). If the current optimization parameter and the minimum optimization parameter indicate the same status (i.e., both succeed or both fail), then the current optimization parameter is set to be the current minimum optimization parameter. Once the optimization parameter has been set, the process will reiterate until the prime criterion parameter converges into the prescribed range.

[0011] In accordance with the present invention, there is provided a method of performing a glitch check on multiple nodes of a simulated circuit. The method comprises determining a current optimization parameter from a maximum optimization parameter and the minimum optimization parameter of the circuit simulation. A prime criterion parameter is calculated based on the optimization parameters. If the prime criterion parameter does converge, then the current optimization parameter is saved as a set up or hold time for the circuit simulation. If the prime criterion parameter does not converge, then the circuit is simulated based on the current optimization parameter and a current prime criterion parameter is calculated based on the circuit simulation. Next, a secondary criterion parameter is checked for all reference nodes. If any secondary criterion parameter among all the reference nodes falls beyond a prescribed limit, then the status of the simulation based on the current optimization parameter is set to fail. Otherwise, the status of the simulation is set to succeed.

[0012] The prime criterion parameter is a bisection error of the circuit simulation. The process will reiterate until the prime criterion parameter converges into a prescribed range. The secondary criterion parameter may be the height of a signal pulse or a metastable time of the signal pulse. The current optimization parameter is set to be the current minimum optimization parameter value when the current optimization parameter and the minimum optimization parameter both indicate the same status (i.e., both indicate succeed or fail). On the other hand, the current optimization parameter is set to be the current maximum optimization parameter value when the current optimization parameter and the minimum optimization parameter do not indicate the same status (i.e., one indicates succeed while the other indicates fail).

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] These, as well as other features of the present invention, will become more apparent upon reference to the drawings wherein:

[0014] FIG. 1 is a flowchart illustrating a reliability-based characterization test using bisection;

[0015] FIG. 2 is a flowchart illustrating a glitch check using signal width;

[0016] FIG. 3 is a flowchart illustrating a glitch check using signal height;

[0017] FIG. 4 is a flowchart illustrating a metastability check;

[0018] FIG. 5 is a flowchart illustrating a glitch check by signal height on multiple reference nodes;

[0019] FIG. 6 is a flowchart illustrating a metastability check on multiple reference nodes;

[0020] FIG. 7 is a flowchart illustrating a glitch check by signal height within limited range; and

[0021] FIG. 8 is a flowchart illustrating a metastability check within a limited range.

DETAILED DESCRIPTION

[0022] Various aspects will now be described in connection with exemplary embodiments, including certain aspects described in terms of sequences of actions that can be performed by elements of a computer system. For example, it will be recognized that in each of the embodiments, the various actions can be performed by specialized circuits or circuitry (e.g., discrete and/or integrated logic gates interconnected to perform a specialized function), by program instructions being executed by one or more processors, or by a combination of both. Thus, the various aspects can be embodied in many different forms, and all such forms are contemplated to be within the scope of what is described. The instructions of a computer program as illustrated in FIG. 1 for performing a reliability-based characterization can be

embodied in any computer readable medium for use by or in connection with an instruction execution system, apparatus, or device, such as a computer based system, processor containing system, or other system that can fetch the instructions from the instruction execution system, apparatus, or device and execute the instructions.

[0023] As used here, a "computer-readable medium" can be any means that can contain, store, communicate, propagate, or transport the program for use by or in connection with the instruction execution system, apparatus, or device. The computer-readable medium can be, for example but not limited to, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, device, or propagation medium. More specific examples (a non exhaustive list) of the computer readable-medium can include the following: an electrical connection having one or more wires, a portable computer diskette, a random access memory (RAM), a read only memory (ROM), an erasable programmable read only memory (EPROM or Flash memory), an optical fiber, and a portable compact disc read only memory (CDROM).

[0024] The present invention generally relates to Applicants' co-pending patent applications: "TIMING SOFT ERROR CHECK", Attorney Docket No. 033994-003; "RELIABILITY BASED CHARACTERIZATION USING BISECTION", Attorney Docket No. 033994-004; and "VERIFICATION AND CHARACTERIZATION OF NOISE MARGIN IN INTEGRATED CIRCUIT DESIGNS", Attorney Docket No. 033994-006, filed concurrently herewith and the entire contents of each application are incorporated herein by reference.

[0025] Referring now to the drawings wherein the showings are for purposes of illustrating preferred embodiments of the present invention only, and not for purposes of limiting the same, Figure 1 is a flowchart illustrating a method of determining an optimized parameter for a circuit simulation. In step 3001, critical-path circuits of full circuits for the circuit simulations are determined for the bisection procedure. The range and precision of the bisection procedure and

clock cycle timing need to be decided. In step 3002, the circuit is simulated based upon an initial optimization parameter (OP). For the reliability-based characterization illustrated in Figure 1, the OP is the setup time or hold time for the circuit. The initial minimum and maximum OP's are determined by user specified information. In step 3003, the primary criteria parameter (PCP) is calculated for the initial minimum OP. The PCP is the bisection error for the setup time or hold time. Once the PCP is calculated, then the circuit is simulated in step 3004 for the initial maximum optimization parameter (OP). In step 3005, the current PCP is then calculated for the initial maximum OP.

[0026] In step 3006, the current minimum OP and the current maximum OP are compared to determine if they both fail or succeed. Specifically, if both the current maximum OP and the current minimum OP both indicate the same status (both succeed or both fail), then the process proceeds to step 3007 where the process ends because of a same sign error. However, if both the current minimum OP and the current maximum OP do not indicate the same status, then the process proceeds to step 3008 where other reliability checks on the circuit may be performed. Specifically, the user has the option of performing glitch and metastability checks C1 – C7.

[0027] Referring to Figure 2, the process for performing a glitch check by signal width from process C1 of Figure 1 is shown. The process begins in step 3102 by determining the current left reference width (LeftRefWidth) and the current right reference width (RightRefWidth) for the signal pulse of the reference node during bisection iteration. Furthermore, the prime criterion parameter (PCP) is determined. For this test, the PCP is the bisection error. The LeftRefWidth, RightRefWidth and PCP is based on the current minimum and maximum values of the optimization parameter which for this test is either the setup time or hold time.

[0028] In step 3103, the current OP value is determined. Specifically, the current OP value is equal to the average of the current minimum OP value and the current maximum OP value. In

step 3104, it is determined whether the PCP (i.e., bisection error) converges. The convergence is determined by whether the bisection error has converged into a bisection precision range which is specified by users. If the convergence has been achieved, then the process proceeds to step 3105 wherein the measurement results are parsed to generate bisection convergence data output and the process ends.

[0029] However, if the PCP does not converge in step 3104, then the process proceeds to step 3106 where the circuit is simulated based on the current value of the optimization parameter (OP) so that the current middle reference width of the signal pulse can be calculated, as well as the current value of the PCP (i.e., bisection error). In step 3107, the LeftRefWidth and the MiddleRefWidth are compared. If they both indicate the same status as either succeeding or failing, then the process proceeds to step 3108 wherein the current OP value is set to the current minimum OP value. The process then proceeds to step 3101 wherein the process proceeds until convergence of the PCP.

[0030] However, if the LeftRefWidth and the MiddleRefWidth do not indicate the same status, then the process proceeds to step 3109 wherein the current OP value is set to be the maximum OP value. Once the OP value has been set in step 3109, the process returns to step 3101 where to repeat the procedure until the PCP converges in step 3104.

[0031] Referring to Figure 1, another check that can be specified in step 3008 is the glitch check by signal height (C2). As seen in Figure 3, the process for determining whether there is a glitch by checking the height of the reference signal is shown. The process is similar to that shown in Figure 2, however, the height of the reference signal is used instead of the width. Accordingly, in step 3202 the current LeftRefDiff, RightRefDiff and PCP (i.e., bisection error) are determined for the current minimum and maximum OP's. For this test, the OP is the setup time or hold time. The LeftRefDiff, RightRefDiff and MiddleRefDiff are the height of the signal

pulse during bisection iteration. In step 3203, the current OP value is calculated as the average of the minimum OP value and the maximum OP value. In step 3204, it is determined whether the PCP converges to a bisection precision range which is specified by the user. If the PCP has converged, then the process proceeds to step 3205 where the measurement results are parsed to generate bisection convergence data output and the process ends.

[0032] However, if the PCP does not converge in step 3204, then the process proceeds to step 3206 where the circuit is simulated based on the current OP found in step 3203. When the circuit is simulated, then the current MiddleRefDiff and PCP values are calculated. In step 3207, the current LeftRefDiff and MiddleRefDiff are analyzed to see if they have the same status. In this respect, the status of both the LeftRefDiff and MiddleRefDiff are checked to see if they are the same (i.e., both fail or succeed). If the status is the same, then the process proceeds to step 3208 wherein the current OP value is set to be the current minimum OP value. The process then returns to step 3201 wherein the procedure is performed again until convergence of the PCP in step 3204.

[0033] If the current LeftRefDiff and MiddleRefDiff do not indicate the same status in step 3207, then the process proceeds to step 3209 wherein the current OP value is set to be the maximum OP value. The process returns to step 3201 wherein the procedure is performed again until convergence of the PCP in step 3204.

[0034] In addition to the foregoing, it is also possible for a metastability check to be performed for characterization. The metastability check assures that there is no metastability or that the metastability is under the specified tolerance. For example, in step 3008 of Figure 1, a metastability check (C3) may be chosen. Referring to Figure 4, the metastability check is performed by determining the current slew time of signal transition during bisection iteration. Specifically, in step 3302, the current LeftSwitchDiff and RightSwitchDiff are determined based

on current minimum OP and maximum OP values. The LeftSwitchDiff and RightSwitchDiff are the slew time of the signal transition. The OP is the optimization parameter of setup time or hold time. Furthermore, the current PCP (i.e., bisection error) is determined in step 3302 for the current maximum and minimum OP values.

[0035] In step 3303, the current OP value is set to be the average of the current minimum and maximum OP values. In step 3304, it is determined whether the bisection error (i.e., PCP) converges into a user defined bisection error precision range. If the PCP has converged into the range, then the process proceeds to step 3305 wherein the measurement results are parsed to generate bisection convergence data output. However, if the PCP does not converge in step 3304, then the process proceeds to step 3306 wherein the circuit is simulated based on the current optimization parameter determined in step 3303. The current MiddleSwitchDiff and the current PCP values are also calculated in step 3306.

[0036] In step 3307, the current LeftSwitchDiff and MiddleSwitchDiff are compared to see if they indicate the same status (i.e., both succeed or both fail). If the LeftSwitchDiff and MiddleSwitchDiff do indicate the same status, then in step 3308 the current OP value is set to be the current minimum OP value and the process returns to step 3301 for further processing. However, if the LeftSwitchDiff and the MiddleSwitchDiff do not indicate the same values, then the current OP value is set to the maximum OP value and the process returns to step 3301.

[0037] It is also possible to use the setup and/or hold time characterization to assure that there is either no glitch or a glitch is under a specified tolerance on multiple reference nodes. Specifically, in step 3008 of Figure 1, a glitch check by signal height on multiple references (C4) can be chosen to be performed. Referring to Figure 5, the current OP is determined by averaging the current minimum and maximum OP's in step 3401. The optimization parameter (OP) is the setup time or the hold time. Next, in step 3410, the PCP (i.e., bisection error) is checked to see if

it converges into a user defined bisection error range. If the PCP does converge, then the current OP is saved for setup and hold time calculations in step 3415. However, if the PCP does not converge in step 3410, then the circuit is simulated in step 3402 based on the current optimization parameter determined in step 3401. Furthermore, the current PCP is calculated in step 3402.

[0038] In steps 3403-3405, all reference nodes are checked to see if there is any node whose measured secondary criterion parameter (SCP), hereby the height of the signal pulse, exceeds a prescribed value. If any such node is found, then the status of the current iteration is considered 'fail'. If no such node is found and the bisection goal is met, then the status of the current iteration is considered to be 'succeed'.

[0039] In step 3406, the status of the current OP and the current minimum OP are compared. If they both indicate the same status (i.e., both succeed or both fail) then the current OP value is set to the current minimum OP value in step 3407. After the value has been set, then the process returns to step 3414 for iteration. However, if the current OP and the current minimum OP do not indicate the same status, then the current OP value is set to the maximum OP value in step 3408 and the process returns to step 3414 for further iterations. In this regard, it is possible to perform a glitch check on multiple reference nodes.

[0040] Similarly, the user has the option to perform metastability checks on multiple reference nodes in step 3008 of Figure 1. Referring to Figure 6, the metastability check on multiple reference nodes is similar to the glitch check for multiple reference nodes described for Figure 5 with the only difference being the secondary criterion parameter is the meta-stable time that is the time that the signal stays in a narrow voltage range (e.g., 0.3*VDD to 0.7*VDD) during the transition.

[0041] For example, referring to Figure 6, in step 3501 the current OP value is determined to be the average of the current minimum and maximum OP values. The OP value is the setup time or the hold time. In step 3510, it is determined whether the PCP (e.g., bisection error) converges into the user-defined bisection error range. If the PCP does converge into the range, then the current OP is saved as the setup or hold time and the process ends. However, if the PCP does not converge, then the circuit is simulated in step 3502 based on the current OP and the current PCP is calculated.

[0042] In steps 3503 – 3505, all reference nodes are checked to see if there is any node with a measured secondary criterion parameter (SCP), hereby the metastable time of the signal transition is the time that the signal stays in a narrow voltage range during the transition, that exceeds a prescribed limit typically within the voltage range of 0.3*Vdd and 0.7*Vdd. If there is any such node found, the status of the current iteration is considered to be 'fail'. If no such node is found and the bisection goal is met, the status of the current iteration is considered to be 'succeed'. In step 3506, the current Op and the current minimum OP values are compared to see whether they both indicate the same status. If they both indicate the same status (i.e., both succeed or both fail) then the current OP value is set to the minimum OP value in step 3507 and the process returns to step 3514 for further iterations. If the current OP and the current minimum OP do not both indicate the same status, then the process proceeds to step 3508 where the current OP value is set to be the maximum OP value. When the current OP value has been set, then the process returns to step 3514 for further iterations.

[0043] Similarly, it is possible to perform a glitch check by signal height with limited range from step 3008 of Figure 1. Referring to Figure 7, the setup and hold time characterization with glitch check by signal height will assure that within a limited range centered by the clock signal transition that there are no glitches or that the glitch is under a specified tolerance. In step 3601,

the current optimization parameter (OP) is determined by averaging the current minimum OP and the current maximum OP. The OP is the setup time or hold time. In step 3611, it is determined whether the PCP (primary criterion parameter) that is the bisection error converges into a defined bisection error range. If the PCP does converge, then in step 3612 the current OP is saved for the setup and hold time calculation.

[0044] In steps 3603-3606, all reference nodes are checked to see if there is any node with a measured secondary criterion parameter (SCP), hereby the height of a signal pulse within a specified measurement range, that exceeds a prescribed value. If any such node is found, then the status of the current iteration is considered 'fail'. If no such node is found and the bisection goal is met, then the status of the current iteration is considered to be 'succeed'.

[0045] In step 3607, the status of the current OP and the current minimum OP are compared to see if they are the same (i.e., both succeed or both fail). If the status is the same, then the process proceeds to step 3608 where the current OP value is set to be the minimum OP value and the process returns to step 3610. If the status of the current OP and the current minimum OP are not the same, then the current OP value will be set the current maximum value and the process returns to step 3610 for further iterations.

[0046] It is also possible to perform a characterization with a meta-stability check with limited range from step 3008 of Figure 1. Referring to Figure 8, the check will assure that there is no metastability or metastability under a specified tolerance for a limited range centered by the clock signal transition. In step 3701 of Figure 8, the current OP (e.g., setup time or hold time) is determined by averaging the current minimum OP and the current maximum OP. Next, in step 3710 the PCP (e.g., bisection error) is checked for convergence into a specified bisection error range. If the PCP converges, then the current OP is saved for the setup and hold time

calculations in step 3711. If the PCP does not converge, then the circuit is simulated based on the current OP in step 3702. The current PCP will also be calculated in step 3702.

[0047] In steps 3703 – 3706, all reference nodes are checked to see if there is any node whose measured secondary criterion parameter (SCP), hereby the meta-stable time of the signal transition within a specified measurement range, exceeds a prescribed value. If any such node is found, then the status of the current iteration is considered to be 'fail'. If no such node is found and the bisection goal is met, then the status of the current iteration is considered to be 'succeed'.

[0048] In step 3707, it is determined whether the status of both the current OP and the current minimum OP are the same. If the status is the same (i.e., they are both succeed or both fail), then in step 3708 the current OP value is set to be the current minimum OP value and the process returns to step 3714 for further iterations. However, if the status is not the same for both the current OP and the current minimum OP in step 3707, then the current Op value will be set to the current maximum OP value in step 3709 and the process will return to step 3714 for further iterations until the PCP converges.

[0049] Referring back to Figure 1, if the user decides not to perform other reliability checks in step 3008, then the process proceeds to step 3009 where the current OP is calculated. Specifically, the current OP is calculated by averaging the current minimum OP and the current maximum OP. After the current OP has been calculated, then the PCP is checked for convergence in step 3010. Specifically, the convergence is determined by whether the bisection error (i.e., PCP) has converged into a bisection precision range which is specified by the user. If the bisection error has converged, then the current OP is saved as the setup and hold time for any subsequent calculations. However, if there is not convergence of the bisection error, then the circuit is simulated again in step 3011 using the current OP calculated in step 3009.

[0050] Once the circuit simulation has been performed, the process proceeds to step 3012 wherein the current OP and the current minimum OP are compared. If both values indicate the same status (i.e., both success or both fail), then the process proceeds to step 3013 wherein the current OP value is set to be the current minimum OP value. Furthermore, the process proceeds to point "A" where in step 3009, the current OP is calculated until convergence occurs.

[0051] However, if in step 3012, the current OP and the current minimum OP values do not indicate the same status, then the process proceeds to step 3014 wherein the current OP is set to be the maximum OP value. Then the process returns to point "A" and step 3009 where the process continues until the bisection error converges. In this respect, the process iteratively repeats to find the optimized setup and hold time.

[0052] It will be appreciated by those of ordinary skill in the art that the concepts and techniques described here can be embodied in various specific forms without departing from the essential characteristics thereof. The presently disclosed embodiments are considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims, rather than the foregoing description, and all changes that come within the meaning and range of equivalence thereof are intended to be embraced.